Amendments to the Specification:

Please replace paragraph [0026] with the following amended paragraph:

$$\ldots, I_k+n+1, I_k+n, I_k+n-1, \ldots, [[I_k+n]]\underline{I_k+1}, I_k, \ldots, I;$$

[0026] I is the instruction ready for execution. I_k is the first queued instruction selected for analysis. According to [[1_x]] $\underline{I_k}$, the last instruction selected for analysis is I_k+n. The resulting latency in the queue is k-i. Based on the flexibility of the clock adjustment circuitry, the number of instructions n and algorithm latency k-i can be chosen to perform clock optimization frequently or in longer periods. A load estimation and clock estimation block 135 takes the collected data and estimates the required microprocessor performance. Based on the load estimation, a clock frequency is selected for clock 140. To reduce processing, instead of analyzing the entire instruction set, a moving average of the instruction's intensity can be taken. The moving average allows for a new load estimate every instruction cycle.

Please replace paragraph [0029] with the following amended paragraph:

[0029] Long term load estimation devices 200, 205, 210 analyze a set of instructions 195 queued off-chip, such as in an off-chip cache or in memory. Based on the long term analysis, the optimum clock estimation device 175 on the IC chip 160 determines a preferred long term clocking frequency for the clock 180. The update of the long term frequency may be performed at the same or a lower rate ~~then~~ than the short term analysis. The optimum clock estimation device 175 also determines the clock frequency for the clock 180 based on the short term analysis

and the preferred long term clocking frequency. Using this two-tier approach, short term performance can be adjusted at a fast rate.